

In the claims:

This listing of claims will replace all prior versions and listings of claims in the application:

- 1 1. (previously presented) An integrated circuit, comprising:
 - 2 an array of memory cells, the array configured as a NAND array in a plurality of
 - 3 columns and rows of memory cells, the columns comprising one or more sets of memory cells in
 - 4 series coupled to a bit line, and the rows comprising sets of memory cells having their respective
 - 5 gate terminals coupled to a word line, memory cells in the array respectively comprising a gate
 - 6 terminal, a first channel terminal, a second channel terminal and a channel region between the
 - 7 first and second channel terminals, a charge trapping structure over the channel region, a
 - 8 tunneling dielectric between the channel region and the charge trapping structure, and a blocking
 - 9 dielectric between the charge trapping structure and the gate terminal;
- 10 circuitry to program the memory cells in the array by E-field assisted tunneling through
- 11 the tunneling dielectric by applying a positive voltage to the gate terminal and a low voltage or
- 12 ground to the first and second channel terminals, while limiting program and erase cycling; and
- 13 circuitry to read data from the memory cells.
- 1 2. (original) The integrated circuit of claim 1, wherein the tunneling dielectric has a barrier
- 2 height and thickness sufficient to prevent direct tunneling.
- 1 3. (original) The integrated circuit of claim 1, wherein the tunneling dielectric has a silicon-
- 2 dioxide equivalent thickness between about 30 Angstroms and about 70 Angstroms.
- 1 4. (original) The integrated circuit of claim 1, wherein the tunneling dielectric comprises silicon
- 2 dioxide, and has a thickness greater than 30 Angstroms.
- 1 5. (original) The integrated circuit of claim 1, wherein the tunneling dielectric comprises silicon
- 2 dioxide, and has a thickness between about 30 Angstroms and about 70 Angstroms.
- 1 6. (original) The integrated circuit of claim 1, wherein the positive voltage is about 15 Volts or
- 2 greater.

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- 1 7. (original) The integrated circuit of claim 1, wherein the E-field is about 15 Volts over 5
- 2 nanometers, or higher.

- 1 8. (original) The integrated circuit of claim 1, wherein said array of memory cells is configured
- 2 as a read only memory.

- 1 9. (original) The integrated circuit of claim 1, wherein memory cells in said array have a negative
- 2 threshold voltage prior to programming.

- 1 10. (original) The integrated circuit of claim 1, wherein memory cells in said array of memory
- 2 cells are configured for one-time programming.

- 1 11. (original) The integrated circuit of claim 1, including a static random access memory array,
- 2 and logic which accesses data stored in said array of memory cells and the static random access
- 3 memory array.

- 1 12. (original) The integrated circuit of claim 1, including a static random access memory array,
- 2 and a processor which executes instructions, including instructions for access to data stored in
- 3 said array of memory cells, and stored in the static random access memory array.

- 1 13. (original) The integrated circuit of claim 1, including a static random access memory array,
- 2 and a processor which executes instructions, including instructions for access to data stored in
- 3 said array of memory cells, and stored in the static random access memory array, and wherein
- 4 said logic to program comprises instructions executed by the processor.

- 1 14. (original) The integrated circuit of claim 1, wherein the charge trapping structure comprises
- 2 silicon nitride.

- 1 15. (previously presented) The integrated circuit of claim 1, wherein the charge trapping
- 2 structure comprises a metal oxide.

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1 16. (original) A read only memory cell, comprising:
2 a first channel terminal;
3 a second channel terminal spaced away from the first channel terminal by a channel, and
4 wherein the channel is configured to have a negative threshold prior to programming;
5 a charge trapping structure;
6 a gate;
7 a blocking dielectric between the charge trapping structure and the gate; and
8 a tunnel dielectric between the channel and the charge trapping layer, wherein the tunnel
9 dielectric has a barrier height and thickness sufficient to prevent direct tunneling, the memory
10 cell adapted for one-time programming by applying a positive voltage to the gate and a low
11 voltage or ground to the first and second channel terminals, and adapted for use as a read only
12 memory.

1 17. (currently amended) An integrated circuit on a single substrate, comprising:
2 an array of memory cells configured as read only memory, the array configured as a
3 NAND array in a plurality of columns and rows of memory cells, the columns comprising one or
4 more sets of memory cells in series coupled to a bit line, and the rows comprising sets of
5 memory cells having their respective gate terminals coupled to a word line, memory cells in the
6 array respectively comprising a gate terminal, a first channel terminal, a second channel terminal
7 and a channel region between the first and second channel terminals, a charge trapping structure
8 over the channel region, a tunneling dielectric between the channel region and the charge
9 trapping structure, and a blocking dielectric between the charge trapping structure and the gate
10 terminal;
11 a plurality of word lines in the array contacting the gates of memory cells in respective
12 rows in the array;
13 a plurality of bit lines in the array coupled to sets of memory cells along respective
14 columns in the array;
15 an address decoder coupled to the plurality of word lines and the plurality of bit lines to
16 address selected memory cells in the array;
17 logic, coupled to the plurality of word lines and the plurality of bit lines, to program the
18 memory cells in the array E-field assisted tunneling of electrons to the charge trapping structure

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19 by applying a positive voltage to the gate terminal and a low voltage or ground to the first and
20 second channel terminals, while limiting program and erase cycling; and
21 sense circuitry, coupled to the plurality of bit lines, to sense threshold voltages in selected
22 memory cells in the array.

1 18. (original) The integrated circuit of claim 17, wherein the tunneling dielectric has a silicon
2 dioxide equivalent thickness between about 30 Angstroms and about 70 Angstroms.

1 19. (original) The integrated circuit of claim 17, wherein the tunneling dielectric comprises
2 silicon dioxide, and has a thickness greater than 30 Angstroms.

1 20. (original) The integrated circuit of claim 17, wherein the tunneling dielectric comprises
2 silicon dioxide, and has a thickness between about 30 Angstroms and about 70 Angstroms.

1 21. (original) The integrated circuit of claim 17, wherein the positive voltage is about 15 Volts or
2 greater.

1 22. (original) The integrated circuit of claim 17, wherein the E-field is about 15 Volts over 5
2 nanometers, or higher.

1 23. (original) The integrated circuit of claim 17, wherein memory cells in said array have a
2 negative threshold voltage prior to programming.

1 24. (original) The integrated circuit of claim 17, wherein memory cells in said array of memory
2 cells are configured for one-time programming.

1 25. (original) The integrated circuit of claim 17, including a static random access memory array,
2 and logic which accesses data stored in said array of memory cells and the static random access
3 memory array.

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1 26. (original) The integrated circuit of claim 17, including a static random access memory array,
2 and a processor which executes instructions, including instructions for access to data stored in
3 said array of memory cells, and stored in the static random access memory array.

1 27. (original) The integrated circuit of claim 17, including a static random access memory array,
2 and a processor which executes instructions, including instructions for access to data stored in
3 said array of memory cells, and stored in the static random access memory array, and wherein
4 said logic to program comprises instructions executed by the processor.

1 28. (original) The integrated circuit of claim 17, wherein the charge trapping structure comprises
2 a layer of silicon nitride.

1 29. (previously presented) The integrated circuit of claim 17, wherein the charge trapping
2 structure comprises a metal oxide.